In the Claims:

Please amend claims 1, 8-9, 12, 19-20, 23, 28, and 30, as indicated below.

1. (Currently amended) A system, comprising:

an instruction cache;

a trace cache including a plurality of trace cache entries; and

a trace generator coupled to the instruction cache and the trace cache;

wherein the trace generator is configured to receive a group of instructions output by the instruction cache for storage in one of the plurality of trace cache entries, wherein the trace generator is configured to detect an exceptional instruction within the group of instructions, and wherein the trace generator is configured to store the exceptional instruction in a different trace cache entry than ~~and to prevent the exceptional instruction from being stored in a same one of the plurality of trace cache entries as~~ any non-exceptional instructions.

2. (Original) The system of claim 1, wherein the trace generator is configured to store instructions in the trace cache in at least partially decoded form.

3. (Original) The system of claim 2, further comprising a retire queue coupled to retire executed instructions, wherein the retire queue is configured to prevent retirement of any instruction fetched from the trace cache until all instructions included in a same trace cache entry as that instruction are ready for retirement.

4. (Original) The system of claim 3, further comprising restart logic configured to monitor a number of cycles elapsed since the retire queue last retired an instruction,

wherein if the number of cycles exceeds a threshold number, the restart logic is configured to flush a processing pipeline executing instructions fetched from the trace cache and to restart execution from the instruction cache.

5. (Original) The system of claim 4, further comprising a dispatch unit configured to dispatch instructions received from the trace cache, wherein the dispatch unit is configured to detect a non-re-executable instruction within a group of instructions received from the trace cache and to provide an indication of the non-re-executable instruction to the restart logic;

wherein in response to the indication, the restart logic is configured to flush the processing pipeline and to restart execution from the instruction cache prior to execution of the non-re-executable instruction.

6. (Original) The system of claim 2, further comprising a dispatch unit configured to dispatch instructions received from the instruction cache, wherein the dispatch unit is configured to detect the exceptional instruction within a group of instructions received from the instruction cache and to provide an indication of the exceptional instruction to the trace generator, wherein the trace generator is configured to detect the exceptional instruction in response to the indication from the dispatch unit.

7. (Original) The system of claim 2, wherein the trace generator is configured to detect the exceptional instruction in response to a characteristic of the exceptional instruction.

8. (Currently amended) The system of claim 2, wherein the ~~trace generator is configured to not store the~~ exceptional instruction is an instruction that causes an interrupt or exception ~~in the trace cache~~.

9. (Currently amended) The system of claim 2, ~~wherein the trace generator is configured to store the exceptional instruction in a different trace cache entry than the one~~

~~or more other instructions,~~ wherein the trace generator is configured to not store any other instructions with the exceptional instruction in the different trace cache entry.

10. (Original) The system of claim 2, wherein the exceptional instruction is a non-re-executable instruction.

11. (Original) The system of claim 2, further comprising a retire queue coupled to retire executed instructions, wherein the retire queue is configured to prevent retirement of any instruction fetched from the trace cache until all instructions included in a same liveness group within a same trace cache entry as that instruction are ready for retirement.

12. (Currently amended) A method, comprising:

receiving a group of instructions for storage in a trace cache entry within a trace cache;

storing one or more instructions included in the group of instructions in the trace cache entry;

detecting an exceptional instruction within the group of instructions; and

in response to said detecting, ~~not~~ storing the exceptional instruction <u>in a different</u> ~~within the~~ trace cache entry <u>than any non-exceptional</u> ~~with the one or more~~ instructions.

13. (Original) The method of claim 12, wherein said storing comprises storing the one or more instructions in the trace cache entry in at least partially decoded form.

14. (Original) The method of claim 13, further comprising preventing retirement of any instruction fetched from the trace cache until all instructions included in a same trace cache entry as that instruction are ready for retirement.

15. (Original) The method of claim 14, further comprising:

monitoring a number of cycles elapsed since retirement of any instruction; and

if the number of cycles exceeds a threshold number, flushing a processing pipeline executing instructions fetched from the trace cache and restarting execution from the instruction cache.

16. (Original) The method of claim 14, further comprising:

detecting a non-re-executable instruction within a group of instructions fetched from the trace cache; and

in response to said detecting the non-re-executable instruction, flushing the processing pipeline and restarting execution from the instruction cache prior to execution of the non-re-executable instruction.

17. (Original) The method of claim 13, further comprising dispatching instructions received from the instruction cache, wherein said detecting the exceptional instruction is performed during said dispatching.

18. (Original) The method of claim 13, wherein said detecting comprises a trace generator detecting the exceptional instruction in response to a characteristic of the exceptional instruction.

19. (Currently amended) The method of claim 13, ~~further comprising not storing~~ wherein the exceptional instruction is an instruction that causes an interrupt or exception ~~in any trace cache entry within the trace cache~~.

20. (Currently amended) The method of claim 13, further comprising ~~storing the exceptional instruction in a different trace cache entry within the trace cache than the one or more other instructions and not storing~~ preventing any other instructions from being stored with the exceptional instruction in the different trace cache entry.

21. (Original) The method of claim 13, wherein the exceptional instruction is a non-re-executable instruction.

22. (Original) The method of claim 13, further comprising preventing retirement of any instruction fetched from the trace cache until all instructions included in a same liveness group within a same trace cache entry as that instruction are ready for retirement.

23. (Currently amended) A computer system, comprising:

a system memory; and

a processor coupled to the system memory, wherein the processor includes:

an instruction cache;

a trace cache including a plurality of trace cache entries; and

a trace generator coupled to the instruction cache and the trace cache;

wherein the trace generator is configured to receive a group of instructions output by the instruction cache for storage in one of the plurality of trace cache entries, wherein the trace generator is configured to detect an exceptional instruction within the group of instructions, and wherein the trace generator is configured to store the exceptional instruction in a different trace cache entry than ~~and to prevent the exceptional instruction from~~

~~being stored in a same one of the plurality of trace cache entries as~~ any non-exceptional instructions.

24. (Original) The computer system of claim 23, wherein the trace generator is configured to store instructions in the trace cache in at least partially decoded form.

25. (Original) The computer system of claim 24, further comprising a retire queue coupled to retire executed instructions, wherein the retire queue is configured to prevent retirement of any instruction fetched from the trace cache until all instructions included in a same trace cache entry as that instruction are ready for retirement.

26. (Original) The computer system of claim 25, further comprising restart logic configured to monitor a number of cycles elapsed since the retire queue last retired an instruction, wherein if the number of cycles exceeds a threshold number, the restart logic is configured to flush a processing pipeline executing instructions fetched from the trace cache and to restart execution from the instruction cache.

27. (Original) The computer system of claim 26, further comprising a dispatch unit configured to dispatch instructions received from the trace cache, wherein the dispatch unit is configured to detect a non-re-executable instruction within a group of instructions received from the trace cache and to provide an indication of the non-re-executable instruction to the restart logic;

wherein in response to the indication, the restart logic is configured to flush the processing pipeline and to restart execution from the instruction cache prior to execution of the non-re-executable instruction.

28. (Currently amended) The computer system of claim 24, wherein ~~the trace generator is configured to not store~~ the exceptional instruction is an instruction that causes an interrupt or exception ~~in the trace cache~~.

29. (Original) The computer system of claim 24, further comprising a retire queue coupled to retire executed instructions, wherein the retire queue is configured to prevent retirement of any instruction fetched from the trace cache until all instructions included in a same liveness group within a same trace cache entry as that instruction are ready for retirement.

30. (Currently amended) A system, comprising:

means for storing a group of instructions in a trace cache entry within a trace cache;

means for detecting an exceptional instruction within the group of instructions; and

wherein in response to said detecting, the means for storing ~~do not~~ store the exceptional instruction ~~within the~~ in a different trace cache entry ~~with the one or more~~ than any non-exceptional instructions.